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L Number	Hits	Search Text	DB	Time stamp
L Number		hutton.in.	USPAT;	2004/07/27 08:15
-	838	nutton.in.		2004/07/27 00:13
İ			US-PGPUB;	1
			EPO; JPO	1
_	4.4	hutton.in. and michael	USPAT;	2004/07/27 09:00
		indecontain and maonata	US-PGPUB;	
			EPO; JPO	
-	3	interconnect adj prediction	USPAT;	2004/07/27 09:53
		,	US-PGPUB;	
			EPO; JPO]
		/#5550700#L#5650404#L#5600105#L#6015306#\\ D		2004/07/27 10:16
-	4	("5550782" "5659484" "5689195" "6215326").P		2004/07/27 10:10
			US-PGPUB;	
			EPO; JPO	
_	318	703/19-20.ccls.	USPAT;	2004/07/27 10:30
	010	, , , , , , , , , , , , , , , , , , , ,	US-PGPUB;	
			EPO; JPO	
			1	0004/07/07 10 06
-	10	703/19-20.ccls. and (partition\$3 and	USPAT;	2004/07/27 10:36
		critical adj path)	US-PGPUB;	
			EPO; JPO	
	4	(702/10-20 cala and /nartition\$3 and	USPAT;	2004/07/27 11:01
_	4	(703/19-20.ccls. and (partition\$3 and	· ·	2004/07/27 11:01
		critical adj path)) and (statistic\$3 and	US-PGPUB;	
		estimat\$3)	EPO; JPO]
_	62	timing near driven near placement	USPAT;	2004/07/27 11:01
		• •	US-PGPUB;	
			EPO; JPO	
				2004/07/27 11:02
-	33	(timing near driven near placement) and	USPAT;	2004/07/27 11:02
		partition\$3	US-PGPUB;	
			EPO; JPO	1
l _	6	((timing near driven near placement) and	USPAT:	2004/07/27 11:02
			US-PGPUB;	2001, 01, 21
		partition\$3) and statistic\$2		
			EPO; JPO	
-	4	(((timing near driven near placement) and	USPAT	2004/07/27 11:05
		partition\$3) and statistic\$2) and		
		estimat\$3		
	CO		USPAT;	2004/07/27 11:07
	62	(timing near driven near placement) or		2004/07/27 11:07
		(timing near driven near compilation)	US-PGPUB;	
			EPO; JPO	
_	33	((timing near driven near placement) or	USPAT;	2004/07/27 11:07
		(timing near driven near compilation)) and	US-PGPUB;	
			EPO; JPO	
		partition\$3	1	0004/07/07 11 00
-	5	(((timing near driven near placement) or	USPAT	2004/07/27 11:08
		(timing near driven near compilation)) and		
		partition\$3) and statistic\$2		
	843	716/2.ccls.	USPAT;	2004/07/29 10:42
-	043	710/2.0013.		2001/01/23 10:12
			US-PGPUB;	
			EPO; JPO	1
-	117	716/2.ccls. and partition	USPAT;	2004/07/29 10:42
		**	US-PGPUB;	
[EPO; JPO	
	20	(716/2.ccls. and partition) and	USPAT;	2004/07/29 10:42
-	28			2003/01/29 10:42
		statistic\$2	US-PGPUB;	
]			EPO; JPO	
l _	26	((716/2.ccls. and partition) and	USPAT;	2004/07/29 12:14
		statistic\$2) and timing	US-PGPUB;	
		Journal of the control	EPO; JPO	1
		716/4		2004/07/20 12:14
-	1404	716/4.ccls.	USPAT;	2004/07/29 12:14
			US-PGPUB;	
į			EPO; JPO	
l _	19	716/4.ccls. and partition and statistic\$2	USPAT;	2004/07/29 12:15
1	1 19	-	US-PGPUB;	=001,01,20 12.10
1		and timing		1
1	1		EPO; JPO	1
] -	16	(716/4.ccls. and partition and statistic\$2	USPAT;	2004/07/29 12:16
1	1	and timing) and delay	US-PGPUB;	1
	1		EPO; JPO	
	2200	716/7 14 colo	1	2004/07/29 12:17
-	2396	716/7-14.ccls.	USPAT;	2004/01/29 12:1/
			US-PGPUB;	
	!		EPO; JPO	
-	1	716/7-14.ccls. and partition and	USPAT;	2004/07/29 12:17
1	1	statistic\$2 and timing and delay and bias	US-PGPUB;	
		ration to the contract that he are detay and Dido	, OO LOLUD,	· ·
			EPO; JPO	

			,	
_	37	1	USPAT;	2004/07/29 12:47
		statistic\$2 and timing and delay	US-PGPUB;	
			EPO; JPO	
-	417	716/16.ccls.	USPAT;	2004/07/29 12:47
			US-PGPUB;	
			EPO; JPO	
-	1	716/16.ccls. and partition and statistic\$2	USPAT;	2004/07/29 12:48
		and timing	US-PGPUB;	
i			EPO; JPO	
-	1067	716/17-18.ccls.	USPAT;	2004/07/29 12:48
			US-PGPUB;	
			EPO; JPO	
_	26	716/17-18.ccls. and partition and	USPAT;	2004/07/29 12:52
		statistic\$2 and timing and delay	US-PGPUB;	
			EPO; JPO	
-	2185	326/39-41.ccls.	USPAT;	2004/07/29 12:52
,			US-PGPUB;	
			EPO; JPO	
-	4	326/39-41.ccls. and partition and	USPAT;	2004/07/29 12:53
		statistic\$2 and timing and delay	US-PGPUB;	
1			EPO; JPO	
-	8711	criticality	USPAT	2004/07/29 12:54
_	919	criticality and timing	USPAT	2004/07/29 12:54
_	435	(criticality and timing) and delay	USPAT	2004/07/29 13:03
	296		USPAT	2004/07/29 13:03
	1,	path		
_	57	(((criticality and timing) and delay) and	USPAT	2004/07/29 13:04
		path) and (FPGA or PLD or ASIC)		
_	26	((((criticality and timing) and delay) and	USPAT	2004/07/29 13:04
		path) and (FPGA or PLD or ASIC)) and		
		statistic\$2		